FIG.1

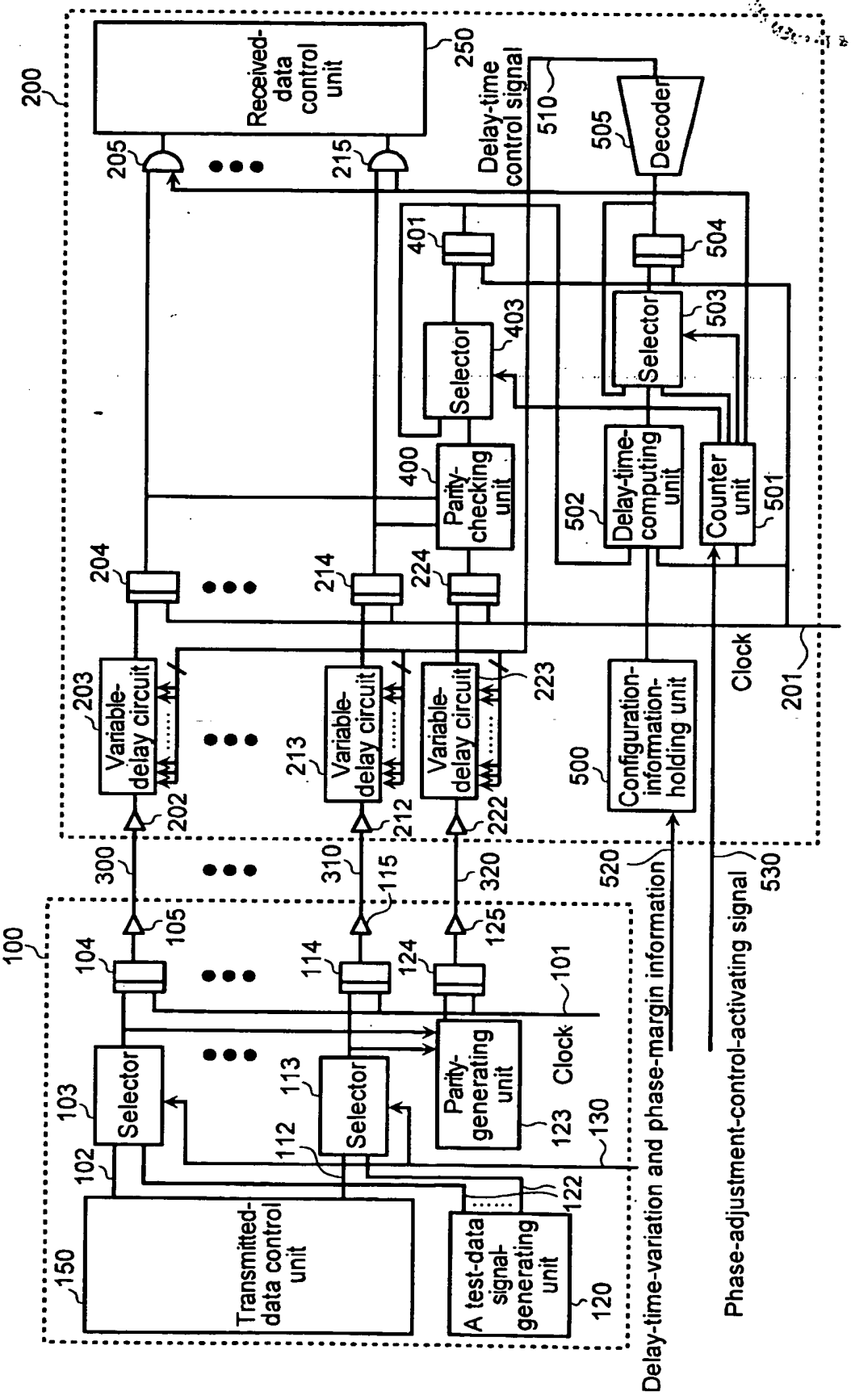
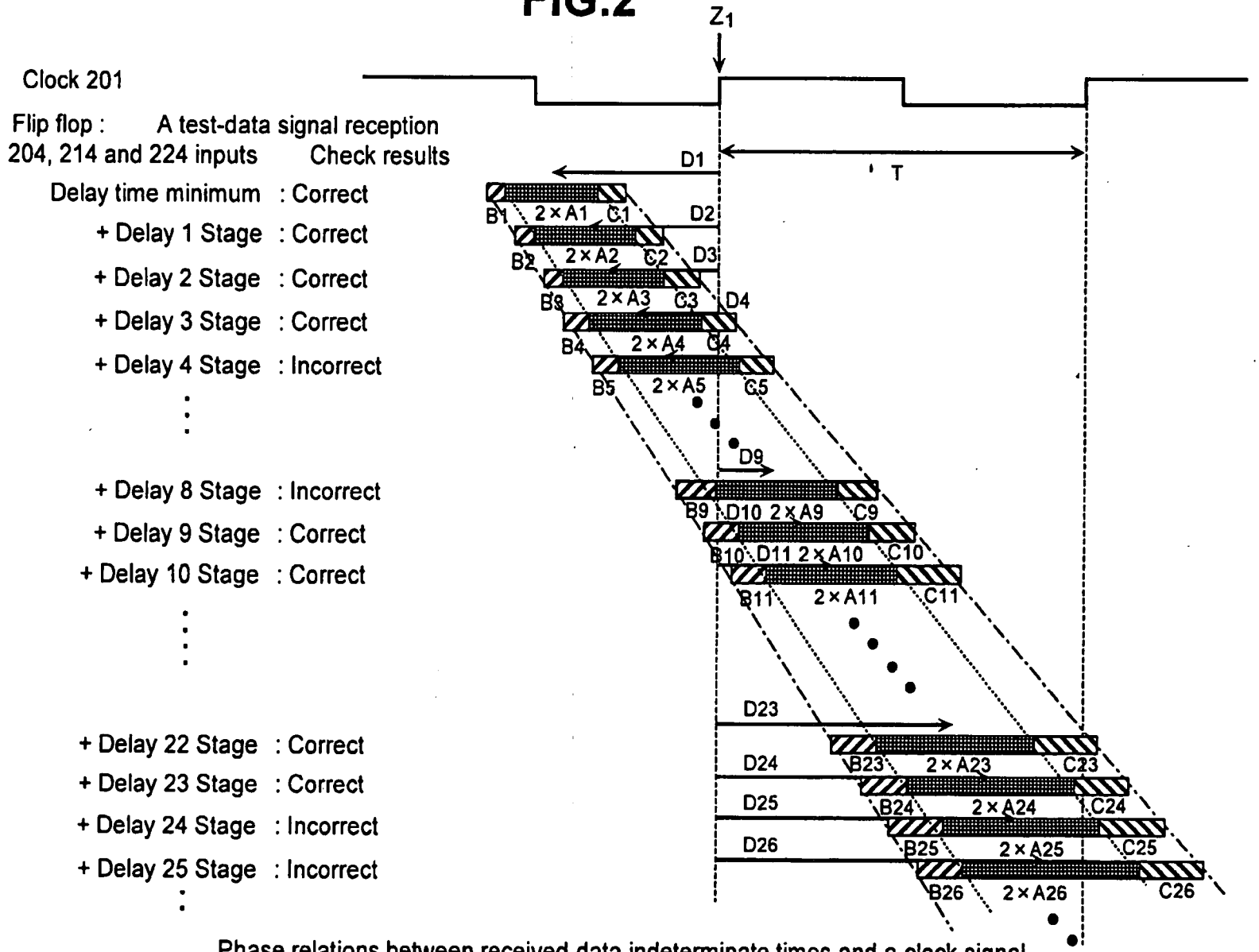
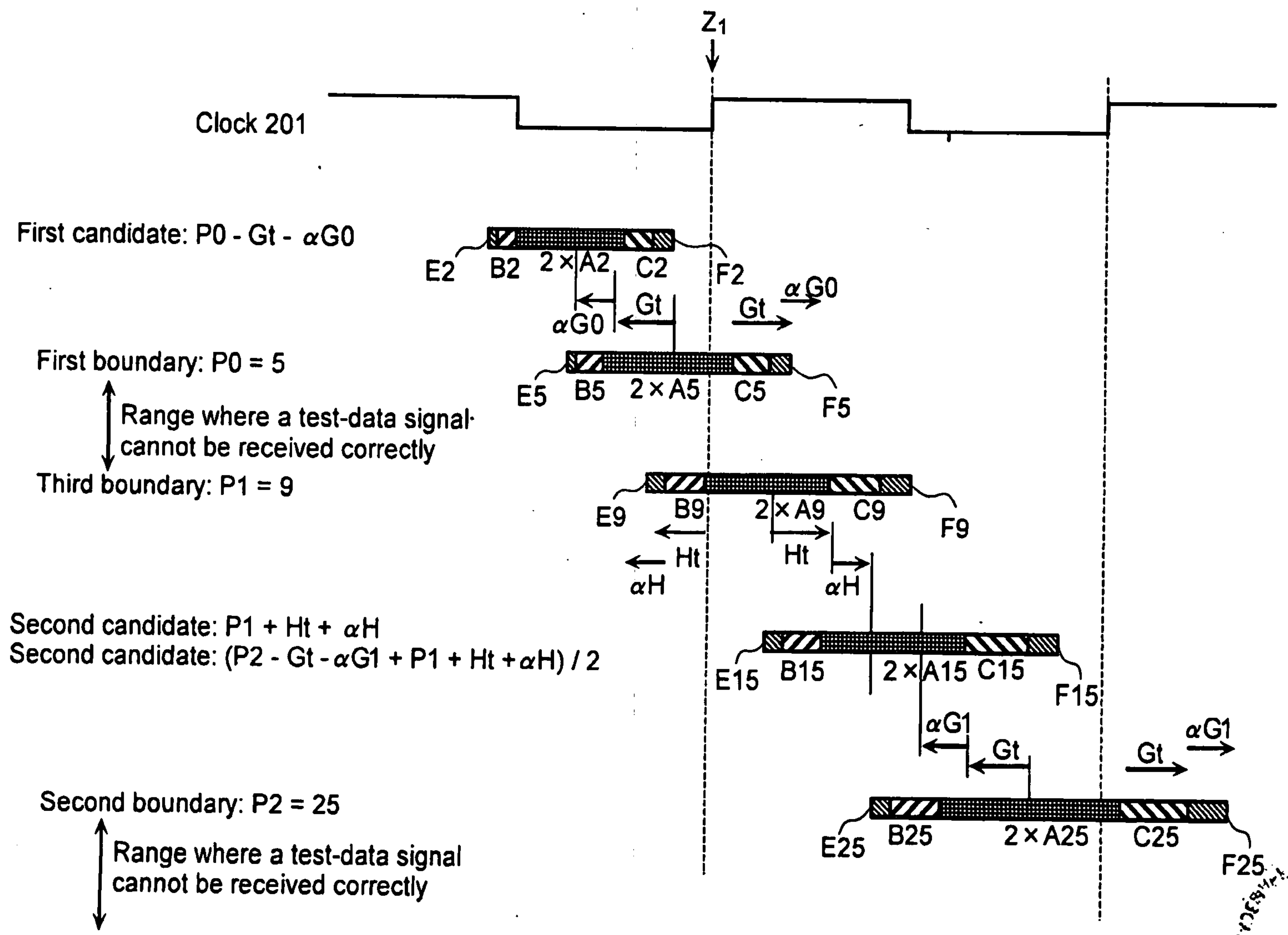


FIG.2



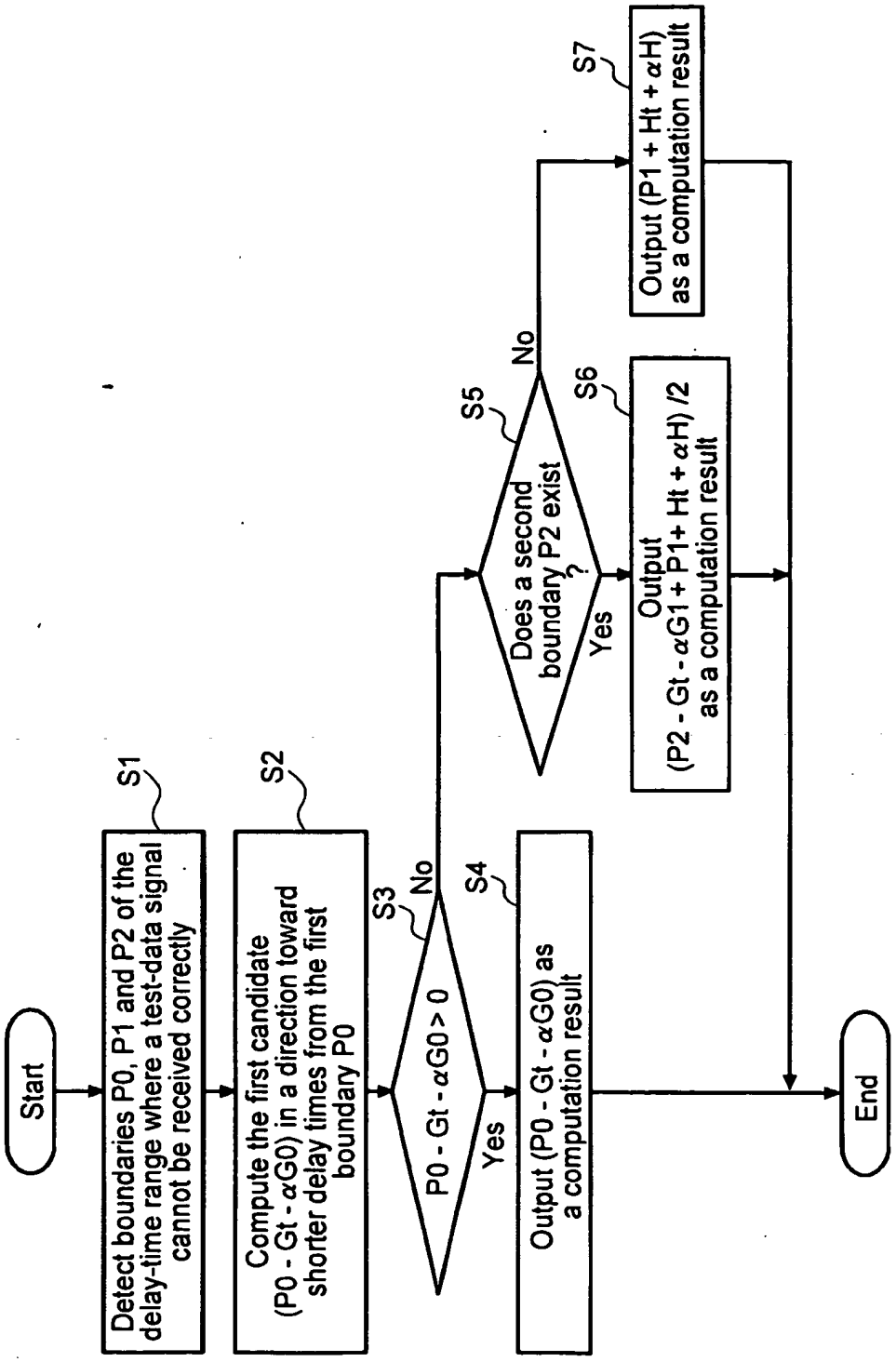
Phase relations between received-data indeterminate times and a clock signal

FIG.3



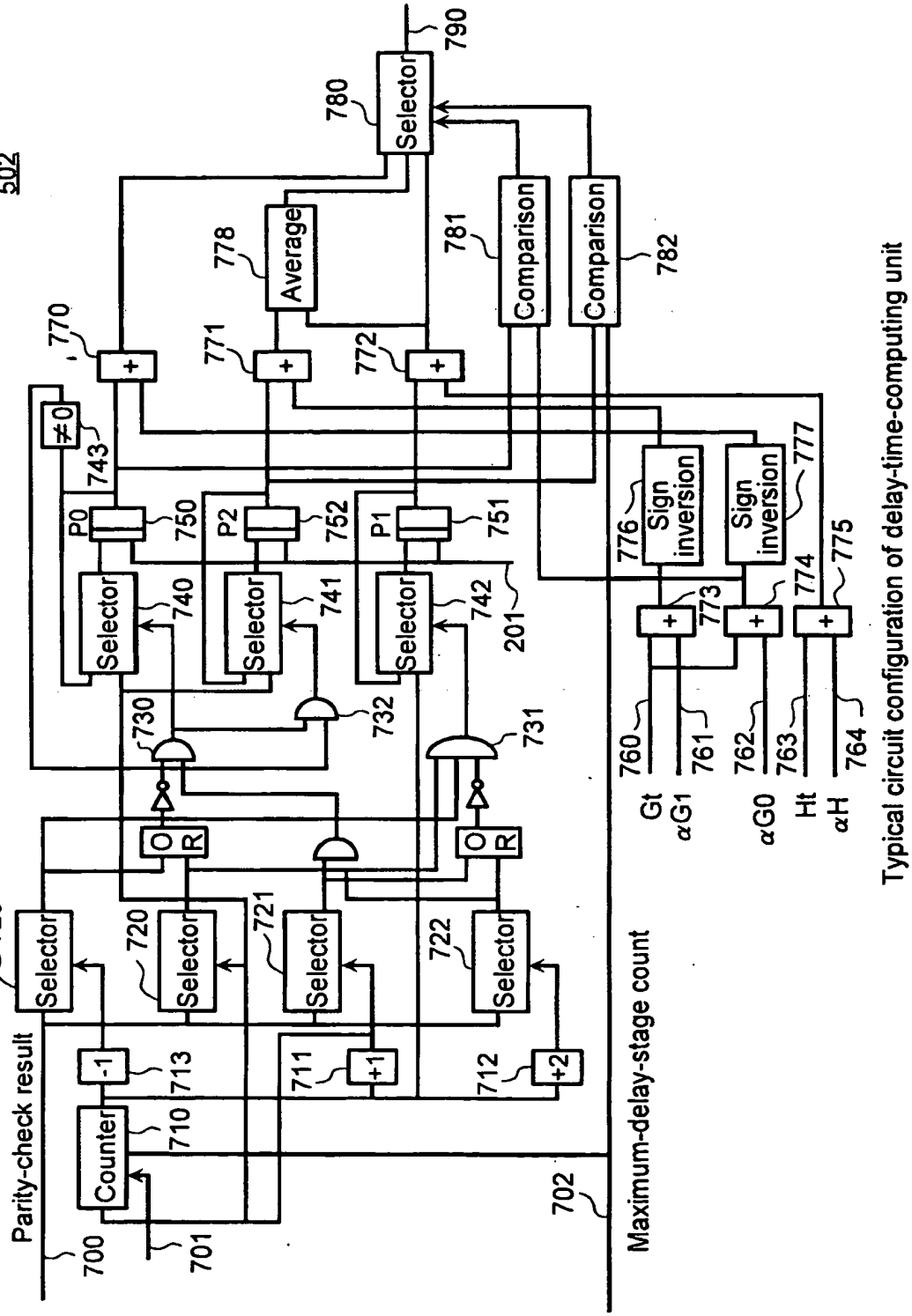
Relations between delay-time variations, external set information and computed delay times

FIG.4



Algorithm of the delay-time computation

FIG.5



Typical circuit configuration of delay-time-computing unit

FIG.6

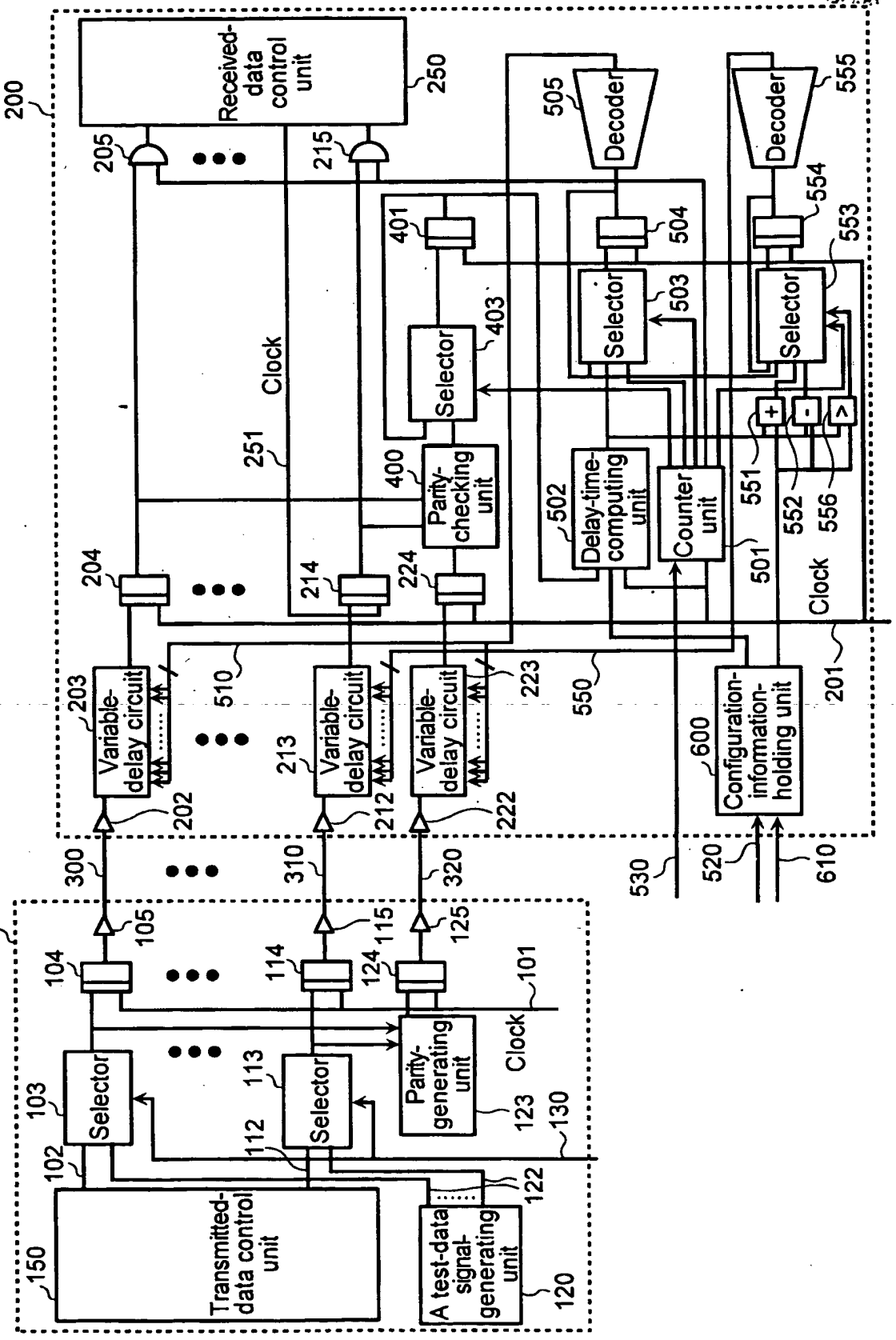

200
Received-data control unit
250
205
215
505
Decoder
555
Decoder
401
504
554
553
Selector
503
Selector
403
Selector
Clock
251
400
Parity-checking unit
502
Delay-time-computing unit
Counter unit
551
552
556
501
204
214
224
Clock
201
203
Variable-delay circuit
510
213
Variable-delay circuit
223
550
Variable-delay circuit
600
Configuration-information-holding unit
202
212
222
300
310
320
530
520
610
100
105
115
125
104
114
124
101
Clock
Parity-generating unit
123
130
Selector
103
113
Selector
112
102
122
Transmitted-data control unit
150
A test-data signal-generating unit
120

FIG.7

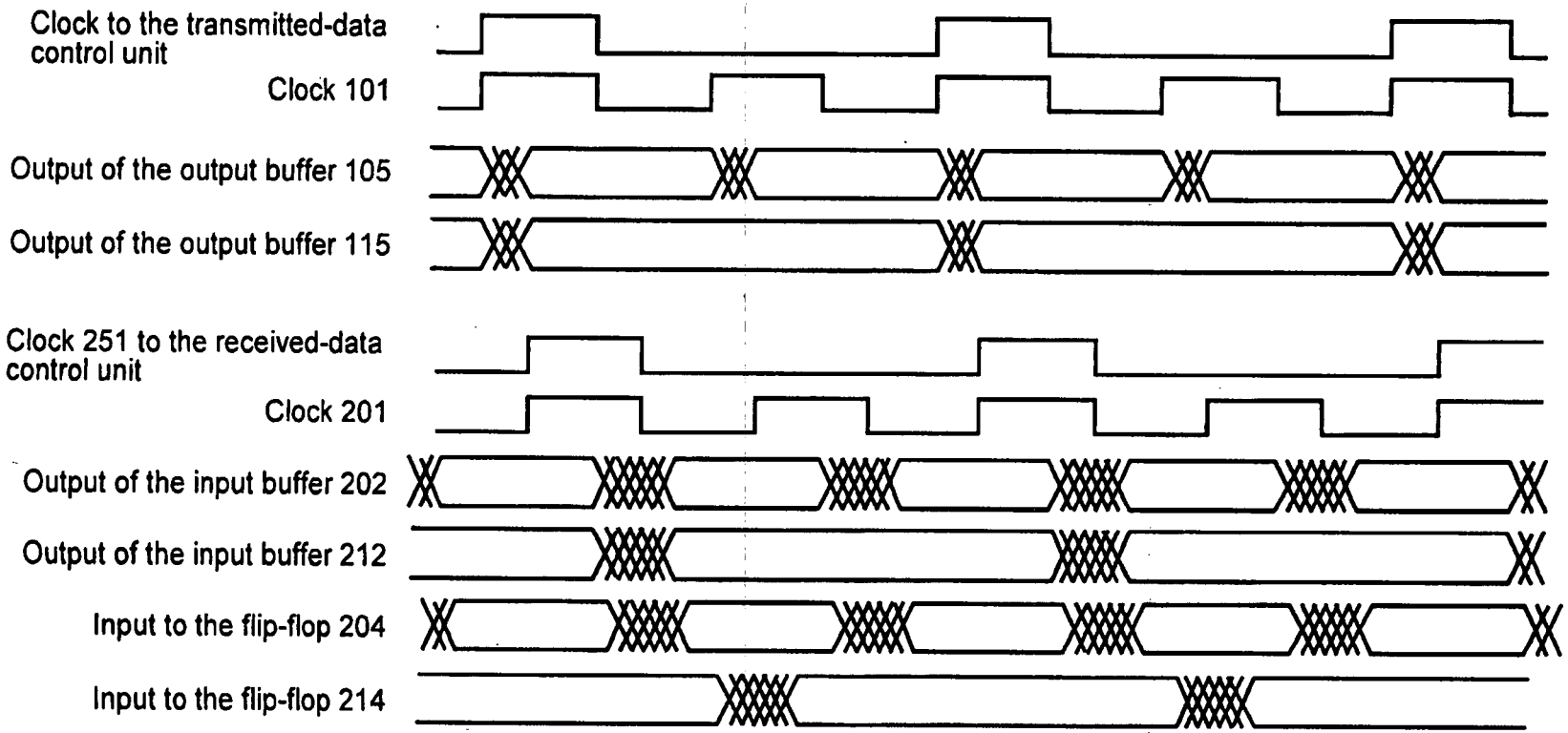


FIG.8

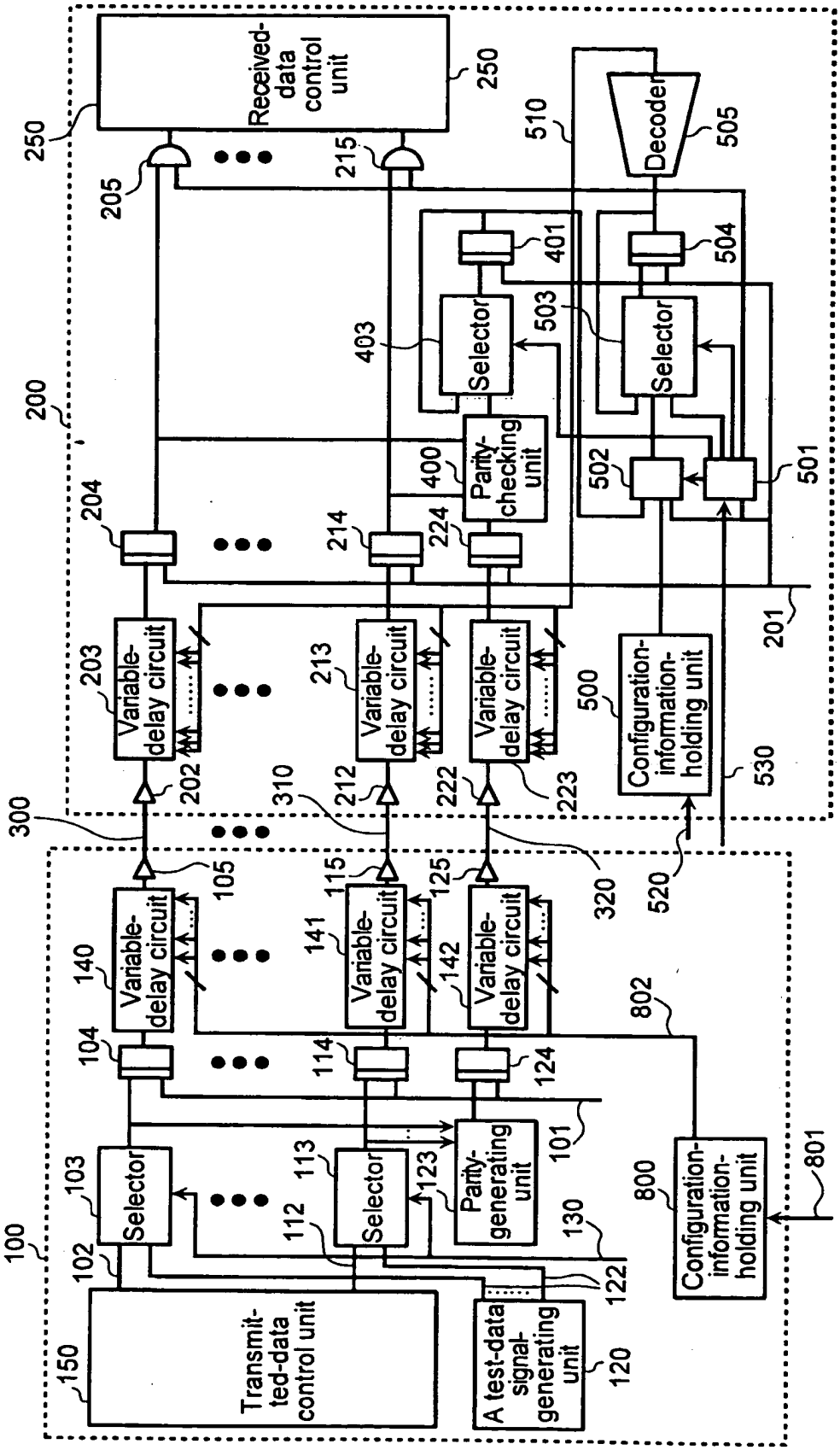
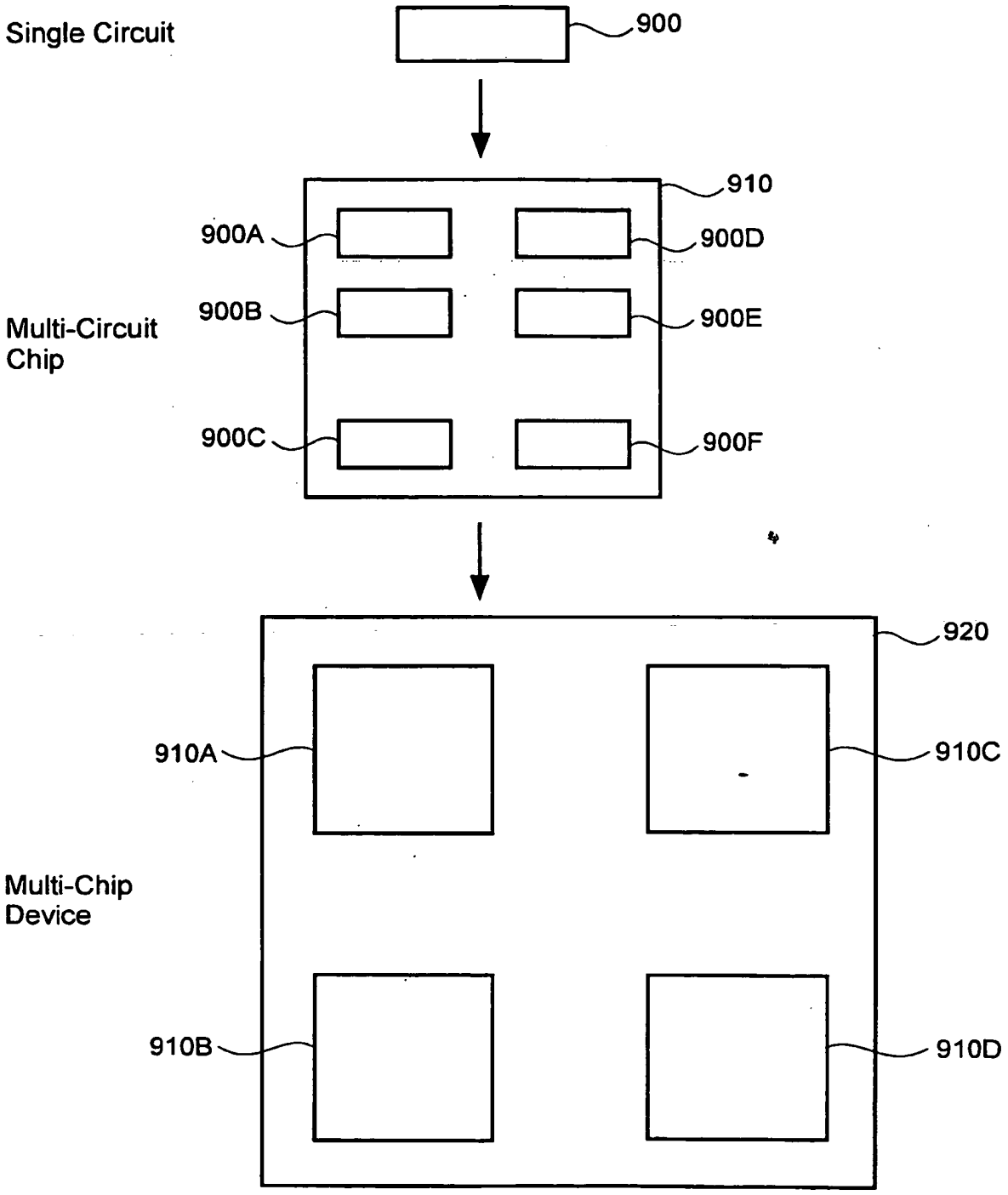

Received-data control unit
250
205
215
Decoder
505
510
401
504
403
Selector
503
Selector
Parity-checking unit
400
502
501
204
214
224
200
201
Variable-delay circuit
203
213
223
500
Configuration-information-holding unit
530
202
310
212
222
300
105
115
125
320
520
140
141
142
802
104
114
124
Selector
103
113
123
Parity-generating unit
101
800
801
Configuration-information-holding unit
100
102
112
130
122
Transmit-ted-data control unit
150
A test-data signal-generating unit
120

FIG.9


Single Circuit
900
910
900A
900D
900B
900E
900C
900F
Multi-Circuit Chip
920
910A
910C
910B
910D
Multi-Chip Device